Consistent Small-Signal and Large-Signal Extraction Techniques for Heterojunction FET's

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***Abstract*— A new method is reported to extract large-signal current and charge sources from the small-signal S-parameters of pseudomorphic heterojunction field effect transistors (PHFET's). This method produces a new intrinsic small-signal equivalent circuit topology with less constraints concerning the extraction of the large-signal current and charge sources. The main advantage of this new topology is charge conservation. The S-parameter measurements of a 0.2-μm PHFET agrees well with the small-signal S-parameter data, obtained after evaluation of the new large-signal model at different bias points.**

I. Introduction

In RECENT years, a large effort has been undertaken to accurately model the characteristics of the active devices used in monolithic microwave integrated circuits (MMIC's). First, linear MMIC functions such as amplifiers have been integrated, requiring broadband small-signal equivalent circuits to optimize the designs. Presently, nonlinear functions such as mixing and frequency multiplication are being integrated, requiring accurate knowledge of the nonlinear characteristics of these active devices.

One of the most popular active devices for integration is the heterojunction field effect transistor (HFET). In order to facilitate circuit design with commercial software, empirical large-signal models are preferred. In this paper we present a method to extract a consistent large-signal model from the small-signal characteristics of a HFET, under the quasi-static assumption. Several large-signal models for MESFET's exist [1]–[5], but for HFET's only a few empirical large-signal models have been published [6], [7]. They are all based on the same small-signal topology (Fig. 1(a)). We propose a new topology with less constraints on the extraction of the large-signal current and charge sources. It is based on the small-signal topology of Fig. 1(b). Charge conservation is the main advantage of this new topology. Another advantage, especially useful in circuit simulators, is that it isn't required to calculate the terminal voltage V_{gd}.

The remainder of this paper concentrates on the intrinsic part of the device, but of course we first have to consider the extrinsic components. These elements, inherent to the geometry of the transistor, are evaluated using the well-known cold modelling technique [8]–[10]. The extrinsic components are in general the parasitic gate and drain capacitances C_{pg} and C_{pd}, source, drain, and gate parasitic resistances R_s, R_d, R_g and inductances L_s, L_d, L_g. The position of these components with respect to the intrinsic circuit is shown in Fig. 1(a) and (b). We suppose that these are independent of gate and drain voltage. They can be subtracted from the measured S-parameters using S-Z and S-Y transformations. So the problem is reduced to the modelling of an intrinsic circuit.

In Section II the basics of consistent large-signal modelling under the quasi-static assumption are reviewed. In the subsequent sections a new equivalent circuit with less components and less stringent conditions is proposed. In the final section, some experimental results of the large-signal extraction techniques for 0.2-μm δ-doped pseudomorphic HFET's are presented.

II. Conditions for Large-Signal Modelling

The principles of consistent large-signal modelling are reviewed here. With a Π-topology, the large-signal circuit is as in Fig. 2(a). This large-signal circuit can be transformed into a small-signal equivalent circuit, but this leads to special conditions between the small-signal components: the integrability conditions. These conditions are necessary to integrate the small-signal (trans)conductances and (trans)capacitances towards the six state variables I_μ and Q_μ with μ being gs, ds and gd, respectively. Detailed information is found in [11]–[14]. The small-signal approximation of the nonlinear π-model is given by:

$$I_\mu(V_{gs}, V_{ds}) = I_\mu(V_{gso}, V_{dso}) + \frac{\partial I_\mu}{\partial V_{gs}} v_{gs} + \frac{\partial I_\mu}{\partial V_{ds}} v_{ds} \quad (1)$$

$$Q_\mu(V_{gs}, V_{ds}) = Q_\mu(V_{gso}, V_{dso}) + \frac{\partial Q_\mu}{\partial V_{gs}} v_{gs} + \frac{\partial Q_\mu}{\partial V_{ds}} v_{ds} \quad (2)$$

where V_{gso} and V_{dso} are the DC bias voltages, v_{gs} and v_{ds} are the small-signal voltage excursions.

If we define

$$\frac{\partial I_\mu}{\partial V_{gs}} = G_{\mu 1} \; \frac{\partial Q_\mu}{\partial V_{gs}} = C_{\mu 1} \quad (3)$$

$$\frac{\partial I_\mu}{\partial V_{ds}} = G_{\mu 2} \; \frac{\partial Q_\mu}{\partial V_{ds}} = C_{\mu 2} \quad (4)$$

then the conditions for consistent large-signal modelling are expressed as follows:

$$\frac{\partial G_{\mu 1}}{\partial V_{ds}} = \frac{\partial G_{\mu 2}}{\partial V_{gs}} \; \frac{\partial C_{\mu 1}}{\partial V_{ds}} = \frac{\partial C_{\mu 2}}{\partial V_{gs}} \quad \forall \mu \in \{gs, ds, gd\} \quad (5)$$

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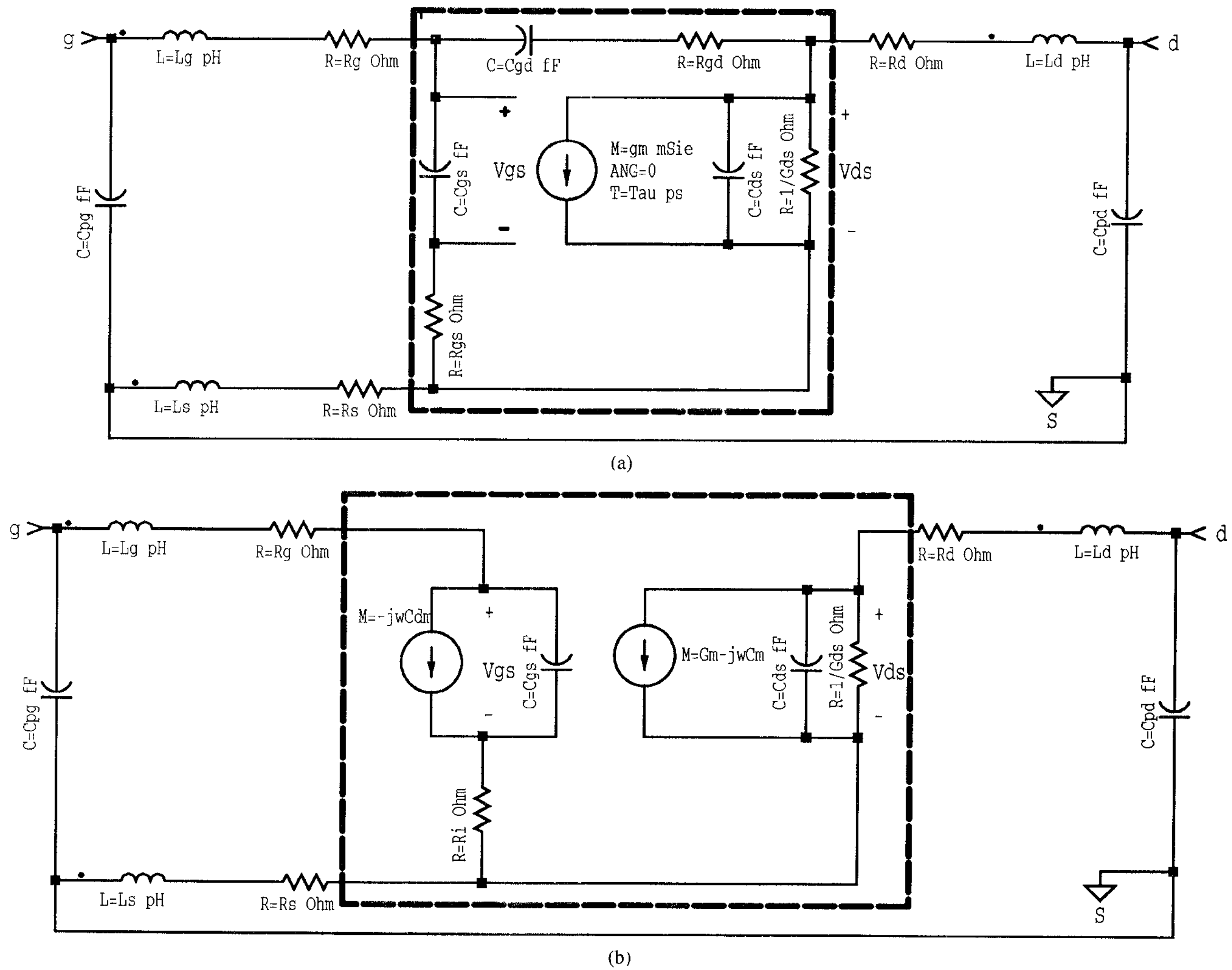

(a)

(b)

Fig. 1. (a) The classical small-signal equivalent circuit for HFET's (b) The new large-signal compatible circuit.

These formulas express the existence of the second derivatives in I_μ and Q_μ. From this derivation it follows that only (trans)conductances and (trans)capacitances can be state variables. So, components that are independent of voltage, like the resistor R_{gs}, have to be banned from the intrinsic large-signal equivalent circuit. By comparison of the Y-matrices of the small-signal approximation of the nonlinear π-model and the conventional small-signal equivalent circuit (Fig. 1(a)) we obtain for the real part:

$$G_{gs1} = 0 \qquad G_{gs2} = 0 \tag{6}$$

$$G_{ds1} = G_m \qquad G_{ds2} = G_{ds} \tag{7}$$

$$G_{gd1} = G_{gd} \qquad G_{gd2} = -G_{gd} \tag{8}$$

and for the imaginary part

$$C_{gs1} = C_{gs} \qquad C_{gs2} = 0 \tag{9}$$

$$C_{ds1} = C_m \qquad C_{ds2} = C_{ds} \tag{10}$$

$$C_{gd1} = C_{gd} \qquad C_{gd2} = -C_{gd} \tag{11}$$

The integrability conditions 5 become:

$$\frac{\partial G_{gd}}{\partial V_{ds}} = -\frac{\partial G_{gd}}{\partial V_{gs}} \qquad \frac{\partial C_{gd}}{\partial V_{ds}} = -\frac{\partial C_{gd}}{\partial V_{gs}} \tag{12}$$

$$\frac{\partial G_m}{\partial V_{ds}} = \frac{\partial G_{ds}}{\partial V_{gs}} \qquad \frac{\partial C_m}{\partial V_{ds}} = \frac{\partial C_{ds}}{\partial V_{gs}} \tag{13}$$

$$\frac{\partial G_{gs}}{\partial V_{ds}} = 0 \qquad \frac{\partial C_{gs}}{\partial V_{ds}} = 0 \tag{14}$$

with

$$G_m = g_m \cdot \cos(\tau) \quad \text{and} \quad C_m = -g_m \cdot \sin(\tau)$$

Best known large-signal models complying with these conditions, are the Curtice Quadratic and Curtice Cubic models [1], [3]. These models, however, do not comply with the accuracy required for large-signal modelling. More precisely, the behavior of the capacitors (charges) is only accurate in a rather small bias range.

III. Large-Signal Compatible Equivalent Circuit

When analyzing the general large-signal circuit, it is obvious that the six state variables $I_{gs}, I_{gd}, I_{ds}, Q_{gs}, Q_{gd}$ and Q_{ds} or the derived small-signal equivalent circuit can never be uniquely defined by the four measured complex S-parameters at each bias point. Therefore, the six state variables of the general circuit will be reduced to four state variables that will be uniquely defined. The standard Π-topology is thereby

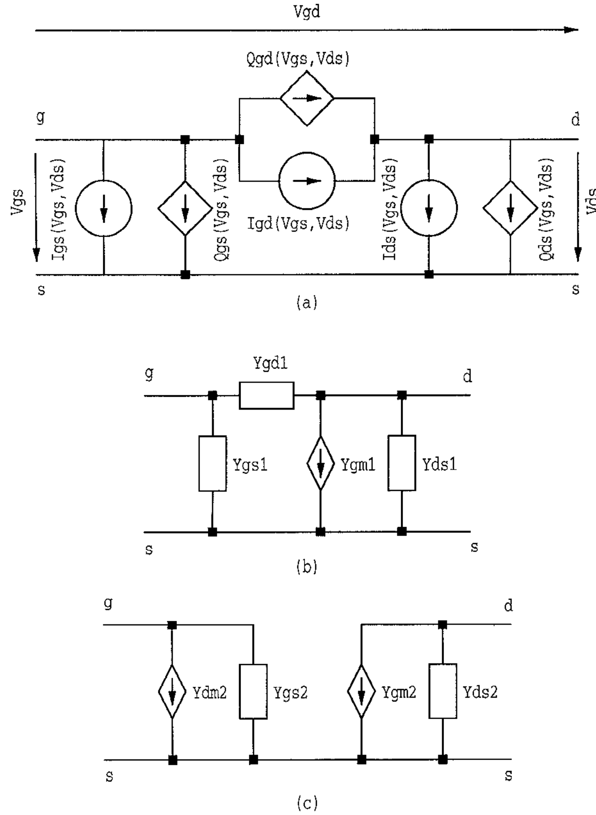

Fig. 2. (a) General Π -topology for large-signal analysis. (b) Topology for the standard small-signal circuit. (c) Newly proposed topology.

changed into two separate circuits with common ground. In Fig. 2(b) and (c), the topology and naming of the components in the circuits are given. Thereby, we will prove that this circuit is at least as general as the standard small-signal equivalent circuit.

From the measured intrinsic Y-parameters, one obtains the small-signal topology of the previous and the new equivalent schemes.

$$Y_{11} = Y_{gs1} + Y_{gd1} \leftrightarrow Y_{11} = Y_{gs2} \tag{15}$$

$$Y_{12} = -Y_{gd1} \leftrightarrow Y_{12} = -Y_{dm2} \tag{16}$$

$$Y_{21} = -Y_{gm1} - Y_{gd1} \leftrightarrow Y_{21} = -Y_{gm2} \tag{17}$$

$$Y_{22} = Y_{ds1} + Y_{gd1} \leftrightarrow Y_{22} = Y_{ds2} \tag{18}$$

Starting from the condition 12 for the gate-drain admittance in the first circuit

$$\frac{\partial Y_{gd1}}{\partial V_{ds}} = -\frac{\partial Y_{gd1}}{\partial V_{gs}}$$

one can prove that

$$\frac{\partial Y_{gs2}}{\partial V_{ds}} = -\frac{\partial Y_{dm2}}{\partial V_{gs}} \Rightarrow \frac{\partial Y_{gs1}}{\partial V_{ds}} = 0$$

and that

$$-\frac{\partial Y_{gm2}}{\partial V_{ds}} = \frac{\partial Y_{ds2}}{\partial V_{gs}} \Rightarrow -\frac{\partial Y_{gm1}}{\partial V_{ds}} = \frac{\partial Y_{ds1}}{\partial V_{gs}}$$

This consistent large-signal circuit is more physical than the circuit of the Curtice and related models because it deals with one gate charge Q_{gs}, depending on gate-source and gate-drain voltage and not with two gate charges, Q_{gs} and Q_{gd}, whose values are rather arbitrarily determined by their position. Consistency problems can occur at $V_{ds} = 0$, when charge is exchanged between Q_{gs} and Q_{gd}, as discussed in [15]–[17]. This can lead to nonconvergence and charge nonconservation.

Finally, the former intrinsic resistances R_{gs} and R_{gd} have to be added. As these resistances together with the series capacitances C_{gs} and C_{gd} are simulating distributed effects, the time constants $R_{gs} * C_{gs}$ and $R_{gd} * C_{gd}$ should be more important than the absolute values. Therefore, the complex ratio of Y_{gs} and Y_{dm} has been calculated as a function of frequency. No frequency dependence is noticed and a real value is calculated as ratio. In the large-signal compatible equivalent circuit, this can be implemented as a resistor R_i added in series with C_{gs} and C_{dm}, both in parallel. The complete equivalent circuit is shown in Fig. 1(b).

The addition of the extrinsic resistor R_i, however, implies that the gate-source current I_{gs} is also modelled externally. This does not increase the complexity of the circuit, although it looks so at first sight.

Finally, the equations to extract the different elements of the new equivalent circuit from the measured intrinsic Y-parameters, using the following conventions, are presented:

$$Y_{gs} = Y_{11} \tag{19}$$

$$Y_{gd} = Y_{12} \tag{20}$$

$$Y_{gm} = Y_{21} \tag{21}$$

$$Y_{ds} = Y_{22} \tag{22}$$

$$ratio = mag\left(\frac{Y_{gd}}{Y_{gs}}\right) \tag{23}$$

$$C_{gs} = \frac{-1}{(\omega * \mathcal{I}(1/Y_{gs}))} \tag{24}$$

$$C_{dm} = C_{gs} * ratio \tag{25}$$

$$C_{ds} = \frac{\mathcal{I}(Y_{ds})}{\omega} \tag{26}$$

$$R_i = \mathcal{R}(1/Y_{gs}) \tag{27}$$

$$R_{gd} = 0 \tag{28}$$

$$G_{ds} = \mathcal{R}(Y_{ds}) \tag{29}$$

$$T_{gs} = R_i * C_{gs} \tag{30}$$

$$G_m = \mathcal{R}(Y_{gm}(1 + j * \omega * T_{gs})) \tag{31}$$

$$C_m = \frac{-1}{(\omega * \mathcal{I}(Y_{gm}(1 + j * \omega * T_{gs})))} \tag{32}$$

This new configuration is simpler than the conventional configuration because we only need to know two internal terminal voltages (V_{gs} and V_{ds}). It is not required to calculate the terminal voltage V_{gd}, which is an advantage to implement this topology in commercial software packages for circuit design, like MDS from Hewlett-Packard and Microwave Harmonica.

IV. Large-Signal Model Extraction

After extraction of the component values according to the large-signal compatible equivalent circuit of Fig. 1(b) from the measured S-parameters at different bias points, one

TABLE I
EXTRINSIC ELEMENTS

	Value	% Std. Dev.
C_{pg} (fF)	24.78	8.7
C_{pd} (fF)	25.64	6.9
L_s (pH)	6.38	-
L_d (pH)	29.18	-
L_g (pH)	34.24	-
R_s (Ω)	2.92	7.5
R_d (Ω)	3.94	4.5
R_g (Ω)	3.00	15.0

has to determine the equations for the four state variables I_{gs}, I_{ds}, Q_{gs}, and Q_{ds} in terms of the internal terminal voltages V_{gs} and V_{ds}. Of course, any physical or empirical function or series expansion can be used. The following empirical curves, based on exponential and hyperbolic functions, serve as an example. They are obtained by extending the physical formulas for DC-curves by several correction terms using the program SIMPAR II [18], which is a parameter extraction and model evaluation software package developed at IMEC.

1) the gate-source diode current

$$I_{gs}(V_{gs}) = a[\exp(bV_{gs}) - 1] \tag{33}$$

2) the source-drain current ′

$$I_{ds}(V_{gs}, V_{ds}) = a \cdot \left[V_{gs} + \frac{1}{b}\ln\cosh(bV_{gs} + cV_{ds} + d) - \frac{1}{e}\exp(eV_{gs} + f) + g\right] \cdot \tanh(hV_{ds}) + iV_{ds} + jV_{ds}^2 \tag{34}$$

3) the gate-source charge

$$Q_{gs}(V_{gs}, V_{ds}) = a\ln\cosh(bV_{gs} + cV_{ds} + d) + e\ln\cosh(fV_{gs}^2 + gV_{gs} + hV_{ds} + i) + jV_{gs} + kV_{ds} + lV_{gs}^2 + mV_{ds}^2 + nV_{gs}V_{ds} + oV_{gs}V_{ds}^2 \tag{35}$$

4) the source-drain charge

$$Q_{ds}(V_{gs}, V_{ds}) = a\ln\cosh(bV_{gs} + cV_{ds} + d) + e\ln\cosh(fV_{gs}^2 + gV_{gs} + hV_{ds} + i) + jV_{gs} + kV_{ds} + lV_{gs}^2 + mV_{ds}^2 + \exp(nV_{gs} + oV_{ds} + p) \tag{36}$$

The diode current I_{gd} was not considered here, but can be added externally. I_{gs} is modelled as a classic diode. No further improvement of the gate diode behavior is required, as further forward biasing generally destroys the device.

These functions for the current and charge sources of the broadband large-signal circuit are suited for simulation of nonlinear microwave analog and transient time domain digital circuits.

TABLE II
SMALL-SIGNAL EXTRACTIONS

	Model 1a		Model 1b	
	Value	% Std. Dev.	Value	% Std. Dev.
g_m (mS)	95.43	0.4	95.34	0.4
C_{gs} (fF)	166.61	2.9	199.73	2.1
C_{gd} (fF)	33.21	4.8	0.00	0.0
C_{dm} (fF)	0.00	0.0	33.19	4.8
G_{ds} (mS)	4.91	1.5	4.95	1.3
C_{ds} (fF)	17.77	24.4	51.03	7.3
R_{gs} (Ω)	2.87	50.7	2.30	42.8
R_{gd} (Ω)	16.84	65.2	0.00	0.0
Tau (pS)	0.78	27.2	0.00	0.0
C_m (fF)	0.00	0.0	110.03	15.3
G_{gs} (mS)	0.00	0.0	0.03	-
G_{gd} (mS)	0.00	0.0	0.00	-
E_{11} %	2.30		2.30	
E_{12} %	4.80		4.90	
E_{21} %	1.50		2.20	
E_{22} %	2.70		4.50	

TABLE III
LARGE-SIGNAL CURRENTS AND CHARGES

	I_{gs} [A]	I_{ds} [A]	Q_{gs} [C]	Q_{ds} [C]
a	5.7E-11	5.2E-02	12.5E-15	-4.3E-15
b	33.9	5.40	4.5	6.7
c		0.18	0.4	0.25
d		0.14	-0.3	0.35
e		4.90	5.7E-15	-8.0E-15
f		-2.70	4.4	3.5
g		0.14	-3.5	-3.4
h		6.00	5.8	5.7
i		4.5E-03	-1.2	-1.2
j		4.7E-04	1.6E-13	1.08E-13
k			-7.9E-14	-9.70E-14
l			-1.7E-14	2.00E-14
m			2.3E-15	-2.80E-15
n			-1.0E-15	7.0
o			5.0E-16	-20.0
p				-33.5

V. EXPERIMENTAL RESULTS

The microwave characteristics of the heterojunction FETs are extracted from S-parameters measurements performed on a HP 8510B Network Analyzer using Tektronix coplanar microwave probes for a frequency sweep from 45–25 GHz. The extracted values for a 0.2 × 100 μm^2 δ-doped pseudomorphic AlGaAs/InGaAs HFET of IMEC, according to the equivalent circuits shown in Fig. 1(a) and (b) can be found in Table I (extrinsic elements) and Table II (intrinsic elements).

The extrinsic components $C_{pg}, C_{pd}, R_s, R_d, R_g, L_s, L_d$ and L_g, have been extracted using the cold modelling technique. For the capacitances and the resistances, the mean value and the relative standard deviation are given in Table I for the

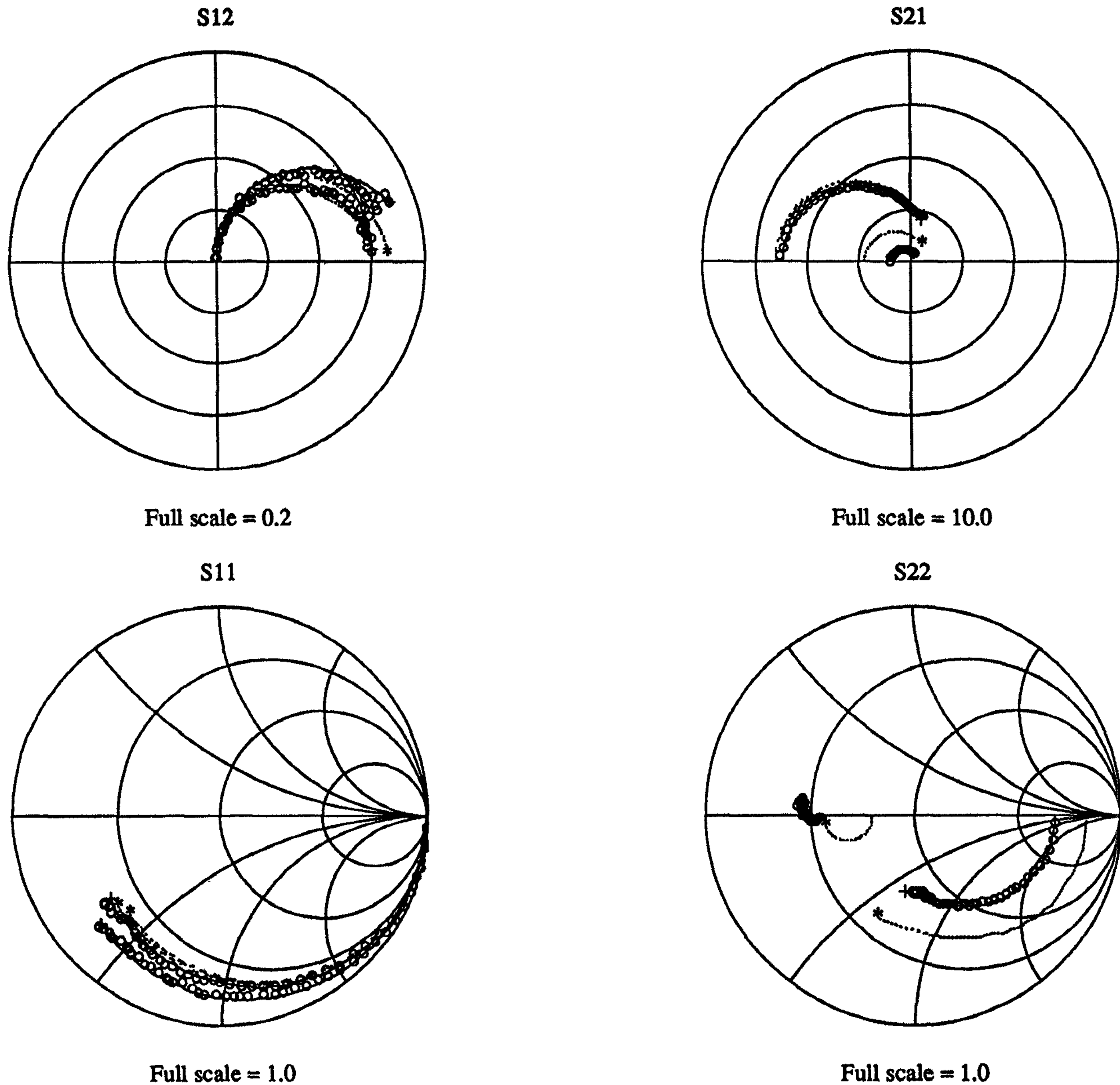

Fig. 3. Measured and fitted S-parameters for a 0.2-μm δ-doped pseudomorphic AlGaAs/InGaAs HFET at bias point V_{gs} = 0.25 V, V_{ds} = 2.00 V, I_{ds} = 30.2 mA and at bias point V_{gs} = 0.20 V, V_{ds} = 0.20 V, I_{ds} = 12.3 mA. ○: measurement —: this paper's model (+ at 25 GHz) ···: Curtice Cubic model (* at 25 GHz)

measured frequency range. As the inductances were found by fitting the admittance as a function of frequency in the band of 5–25 GHz, only best fit values are listed. For the intrinsic components (Table II), the mean value and relative standard deviation are listed. Lower spread for the component values as a function of frequency is obtained for the large-signal compatible equivalent circuit than for those of the classic topology (Fig. 1(b)).

The error terms E_{11}, E_{12}, E_{21} and E_{22} represent the mean relative distance over all frequencies between the measured S-parameters and the ones simulated by the two equivalent circuits. A graphical comparison between the S-parameters calculated from the large-signal compatible equivalent circuit and the measured values is presented in Fig. 3. It can also be seen that the Curtice Cubic model does not comply with the accuracy required for small signal modelling at low V_{ds}.

The nonlinear large-signal current and charge sources are obtained by fitting the extracted small-signal components towards the functions 33 to 36, listed above. This fitting was performed using SIMPAR II. The values of the parameters of the current and charge functions can be found in Table III. Fig. 4 shows a comparison of the G_m-curve fitted by the Angelov model [7] and by our model. In order to design nonlinear circuits based on this model, a good fit in the nonlinear region of the G_m-curve is required. Therefore, a lot of terms in the series expansion of the Angelov-model have to be used, which results in a bad fit of the G_m-curve at maximum G_m. The new proposed formula for the G_m-curve, which is the first

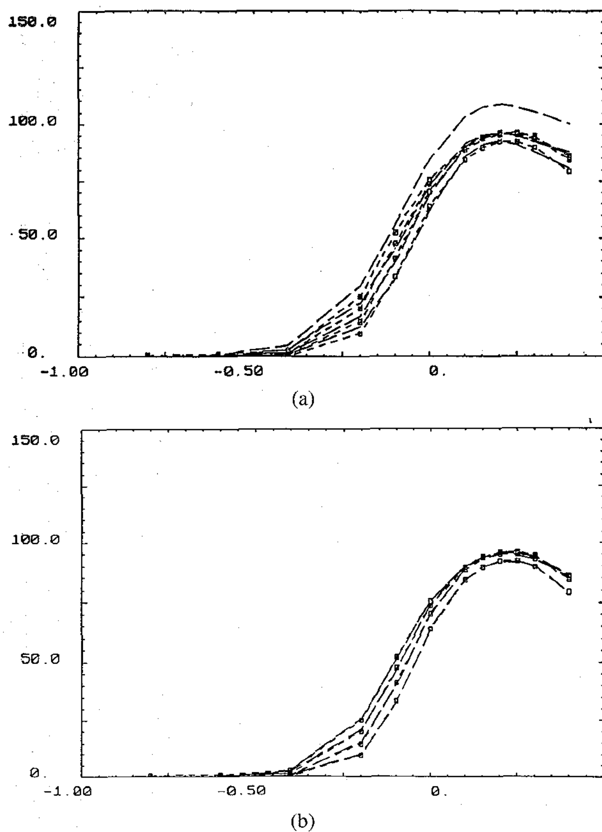

Fig. 4. Comparison of the G_m-curve [mS] in function of V_{gs} [V], using Angelov's model (a) and the new proposed model (b) with measurement data (□).

derivative of the I_{ds}-curve to V_{gs}, fits well the G_m-curve over the whole V_{gs} region.

This consistent large-signal model was succesfully implemented as a symbolically defined device in the Hewlett Packard computer aided design program 'Microwave Design System'.

VI. Conclusion

The analysis of the principles of large-signal modelling leads to the definition of a new small-signal equivalent circuit, consistent with the modelling of large-signal current and charge sources under the quasi-static assumption. The main advantage of this new topology is charge conservation.

A possible implementation of this broadband large-signal model, suited for simulation of nonlinear microwave analog and transient time domain digital circuits, is presented using hyperbolic and exponential functions.

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